

*IEEE P1581*  
*New Possibilities For Static*  
*Component Interconnection Test*

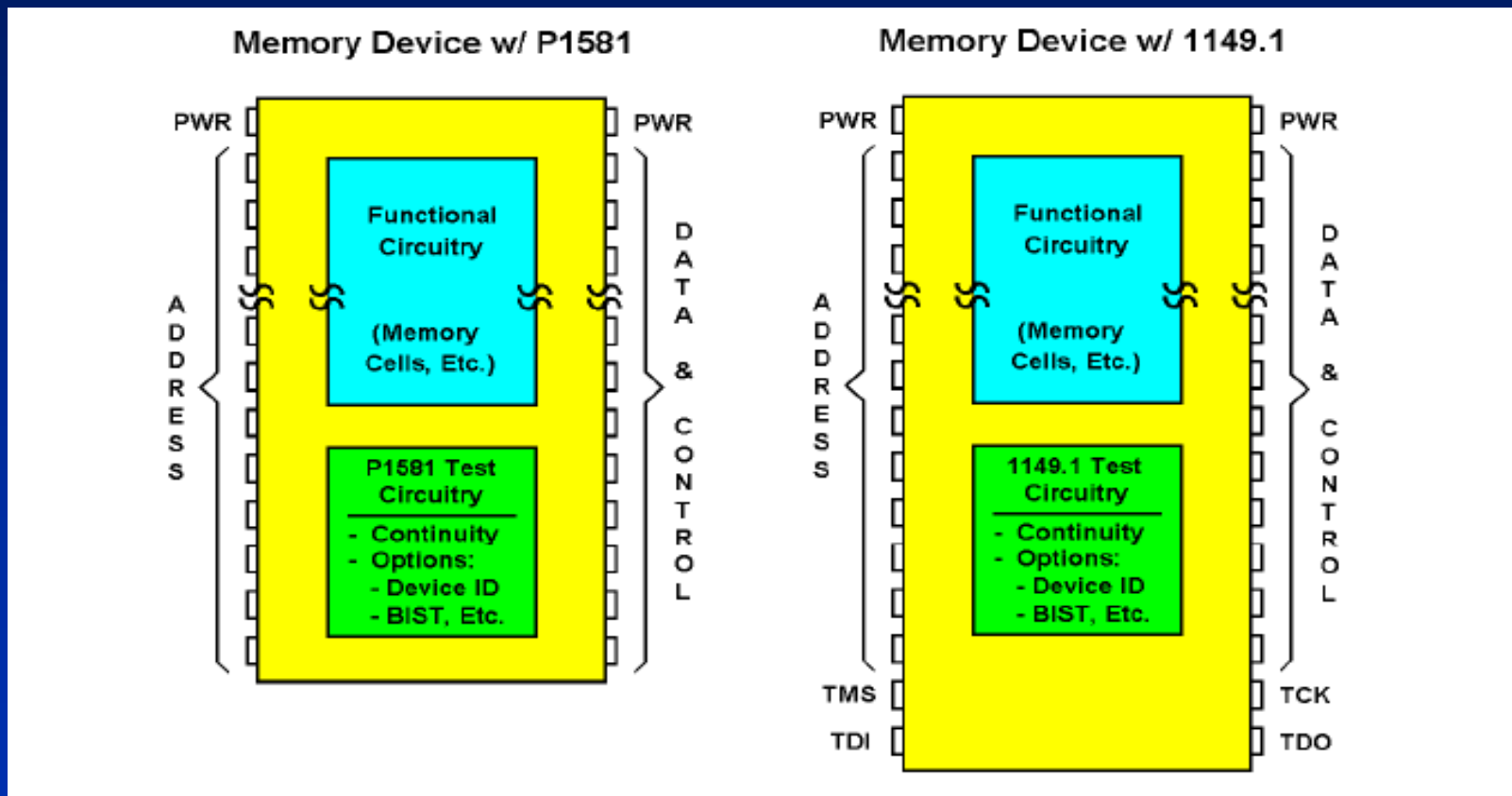
**Scott Creekpaum, ASSET Intertech**

# Outline

- Main features of IEEE P1581
- How can P1581 be used ?
- Who benefits from IEEE P1581 ?

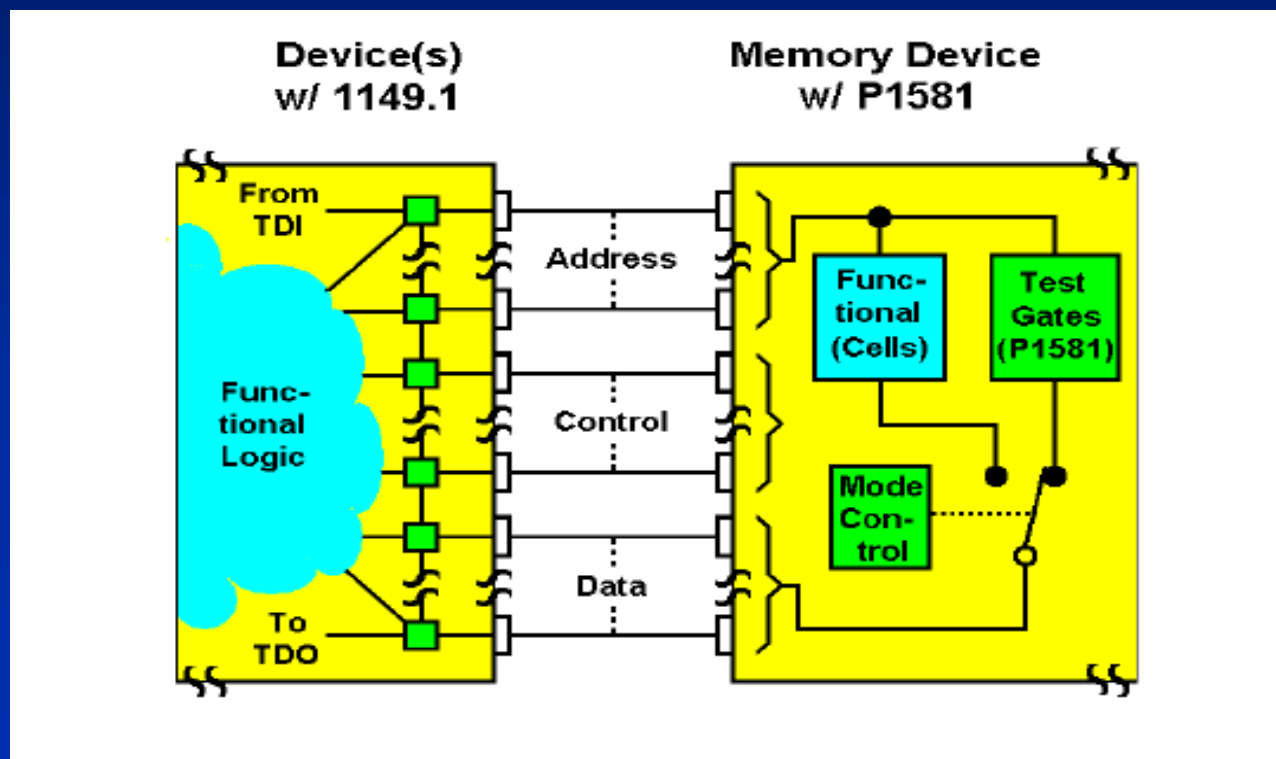
# Main features of IEEE P1581

- Test mode entry and exit do not require extra device pins (*optional test pin is permitted*)



# Main features of IEEE P1581

- Built-in test logic connects inputs to outputs, bypasses memory cells
- No special dynamic requirements

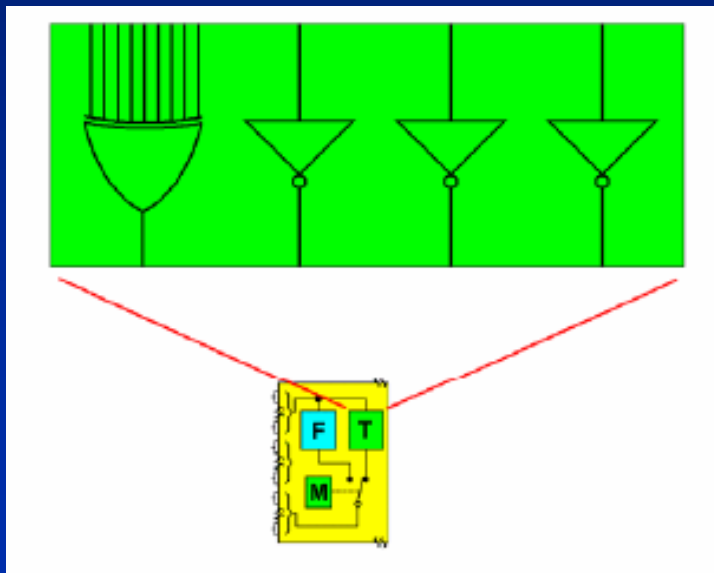


# Main features of IEEE P1581

- Built-in test logic connects inputs to outputs, bypasses memory cells

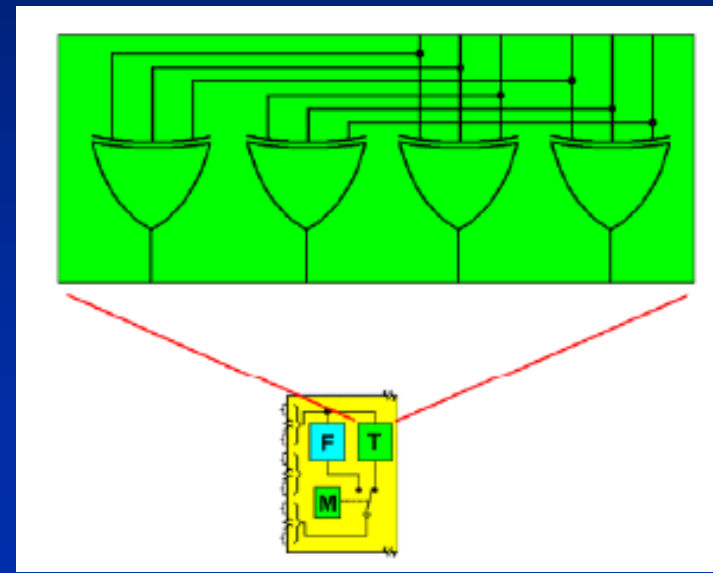
IAX Test Logic

(12 address, 4 data bits)



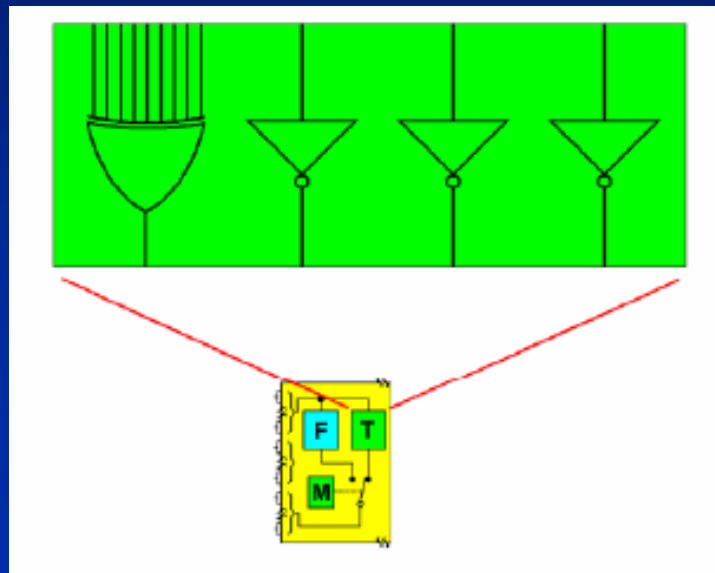
XOR Test Logic

(6 address, 4 data bits)



# Main features of IEEE P1581

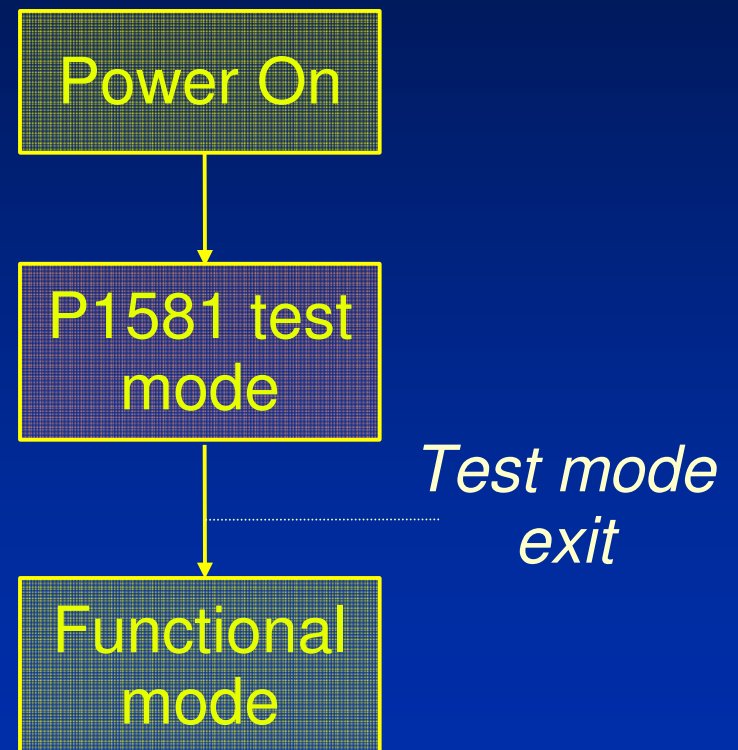
- Very simple test pattern
  - For 12 address bits, complete test could be 26 patterns (all 1's, all 0's, walking 1, walking 0)



# Test mode entry / exit methods

## (Enhanced) Transparent Test Mode method A:

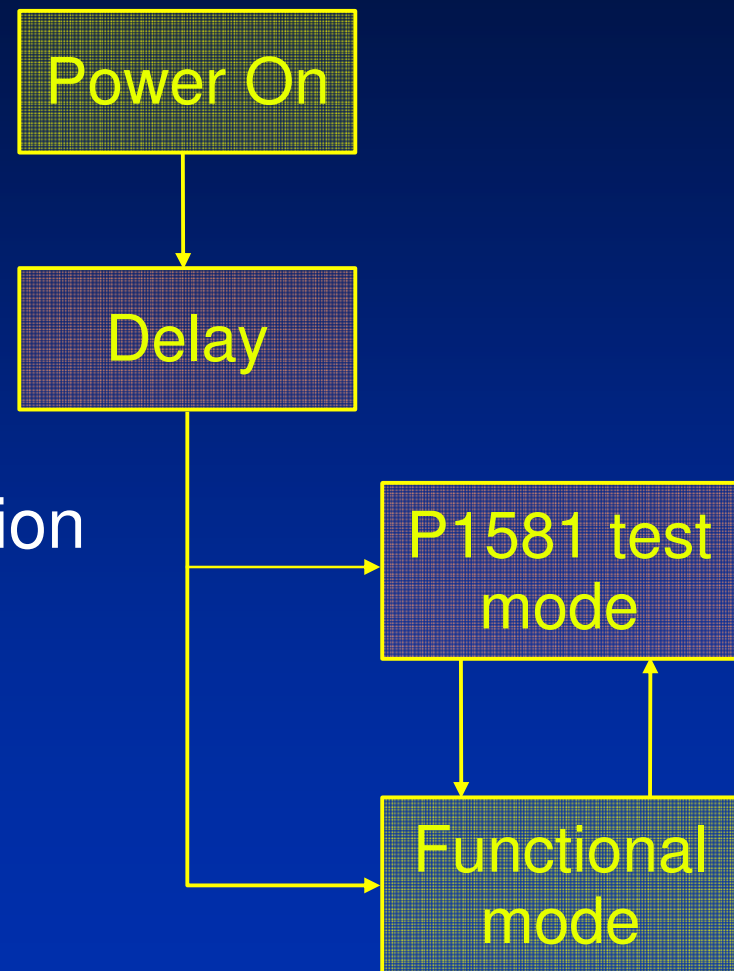
- Device powers up into P1581 test mode
- Exit with first write access after setup time
- Suitable in volatile memory devices



# Test mode entry / exit methods

## TTM method B:

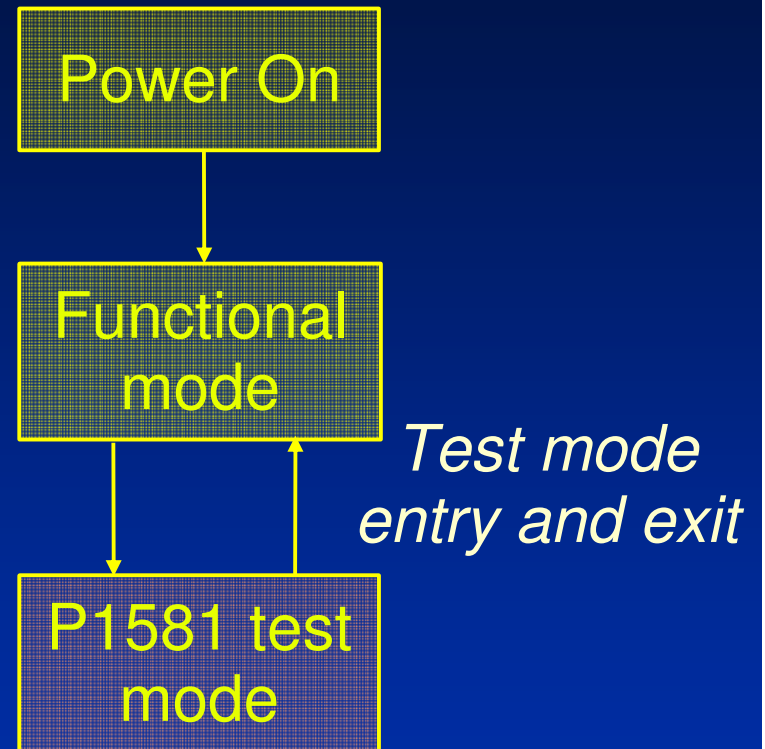
- Delay guarantees stable logic levels on device pins
- Mode selected by input pin state combination after delay
- Exit / Reactivation upon “command”



# Test mode entry / exit methods

## TTM method C:

- Test mode entry / exit by means of:
  - Specific stimulus
  - Clock frequency shifting
  - Analog level shift
  - ...



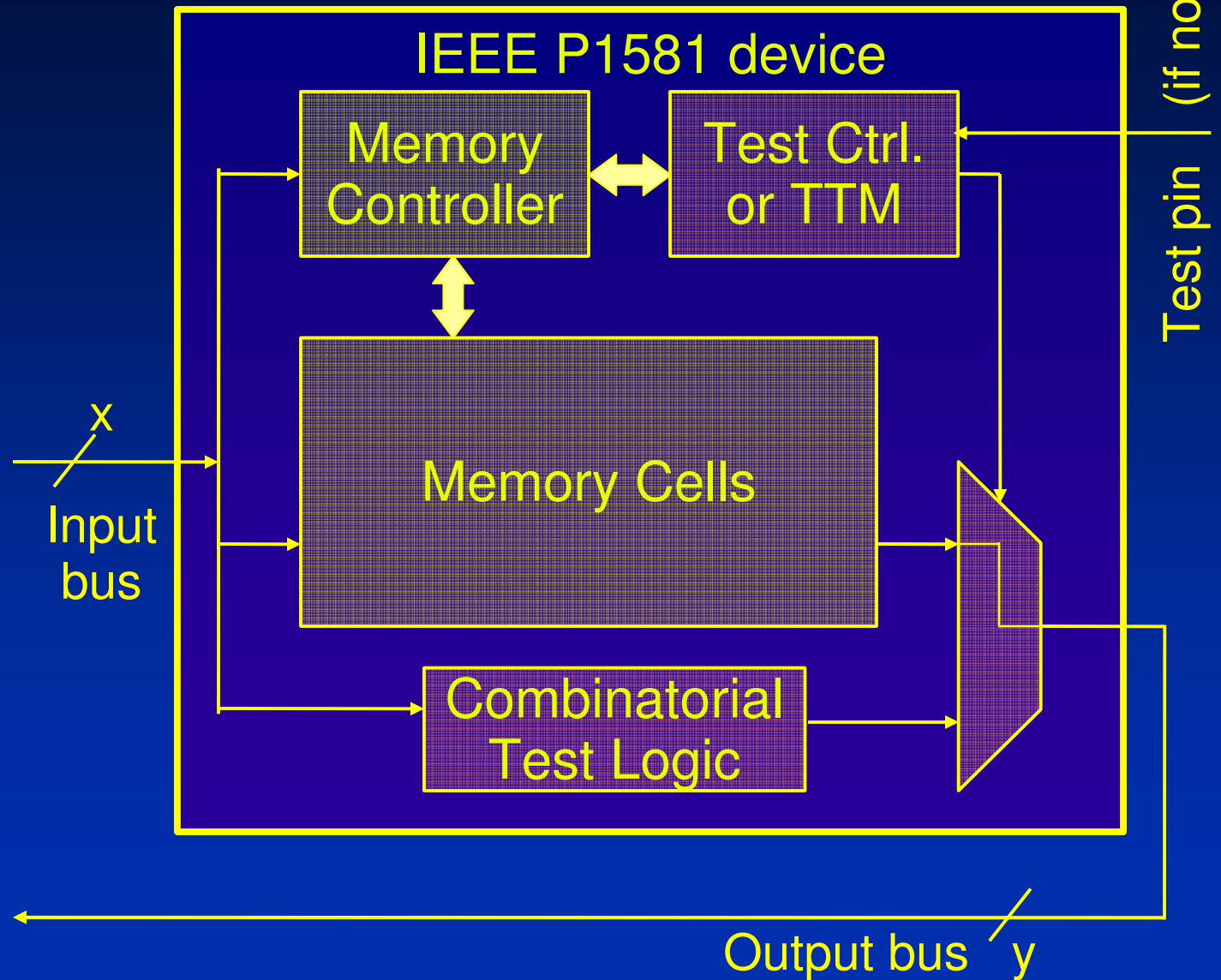
*Primary focus of current WG activities*

# P1581 beyond continuity test

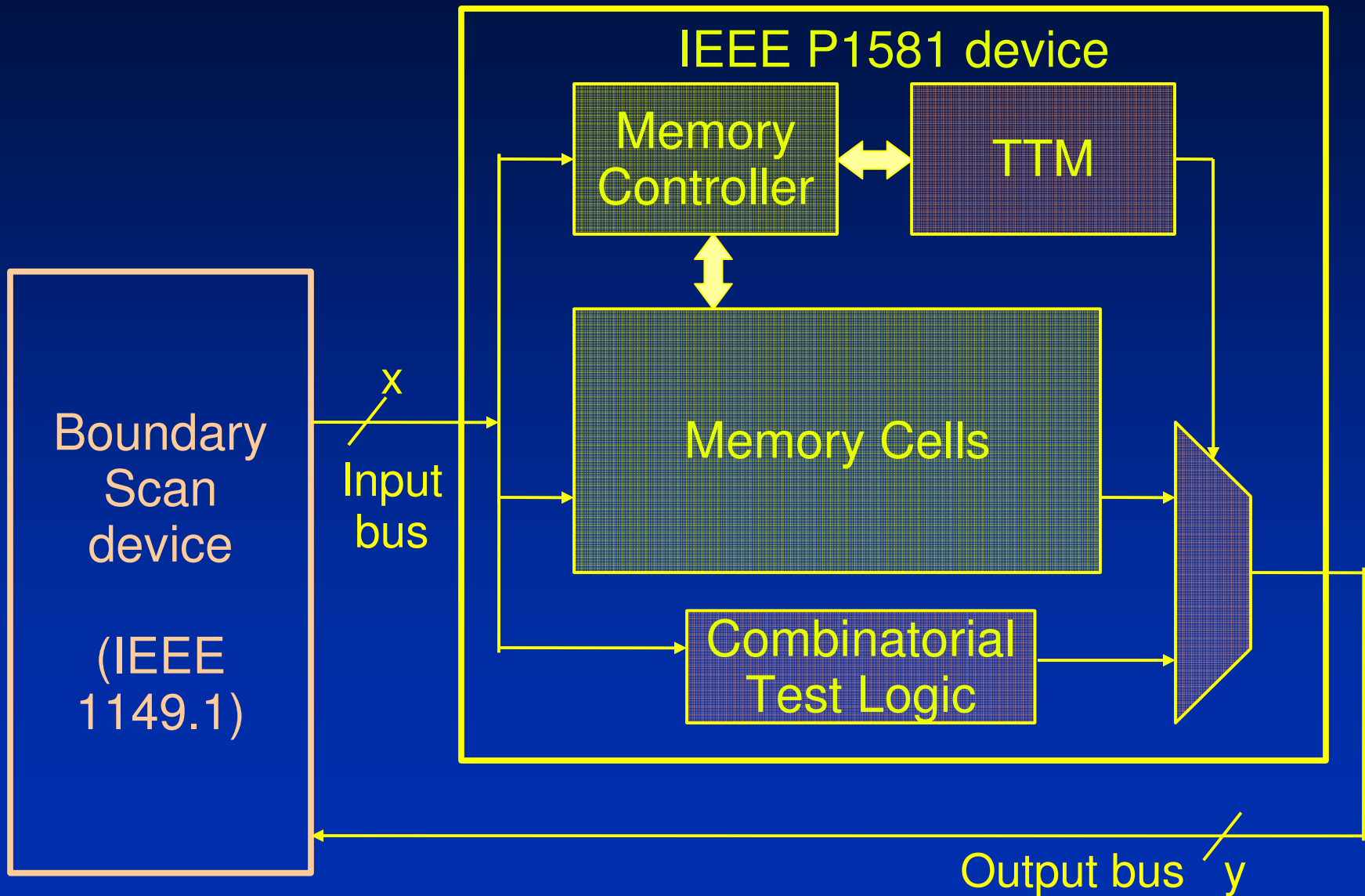
- Continuity test (mandatory)
- Access to device ID
- Self repair
- Built-In Self Test
- Other

# IEEE P1581 principle

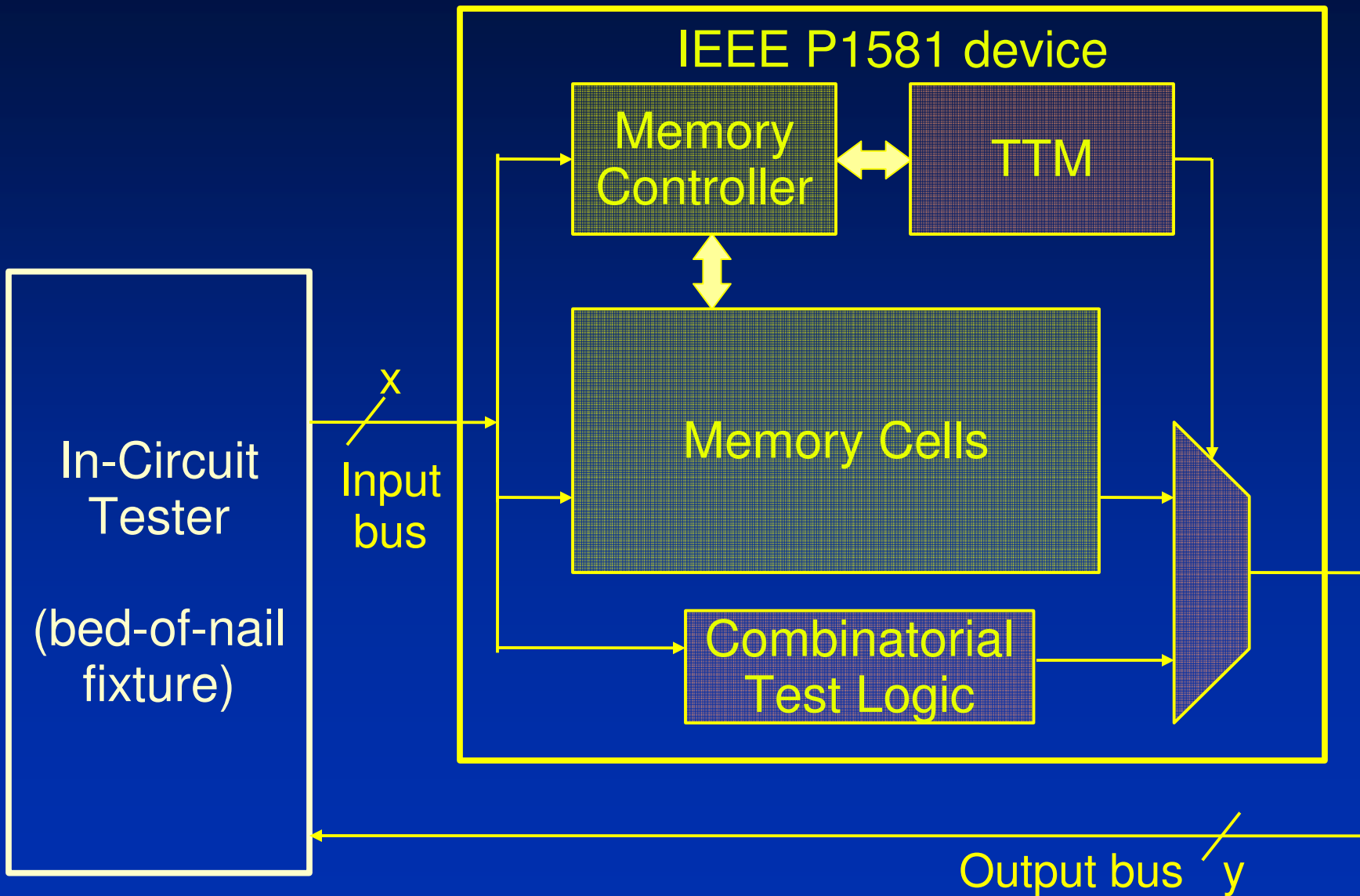
External access to  
memory device pins  
(e.g. from Boundary Scan  
device pins)



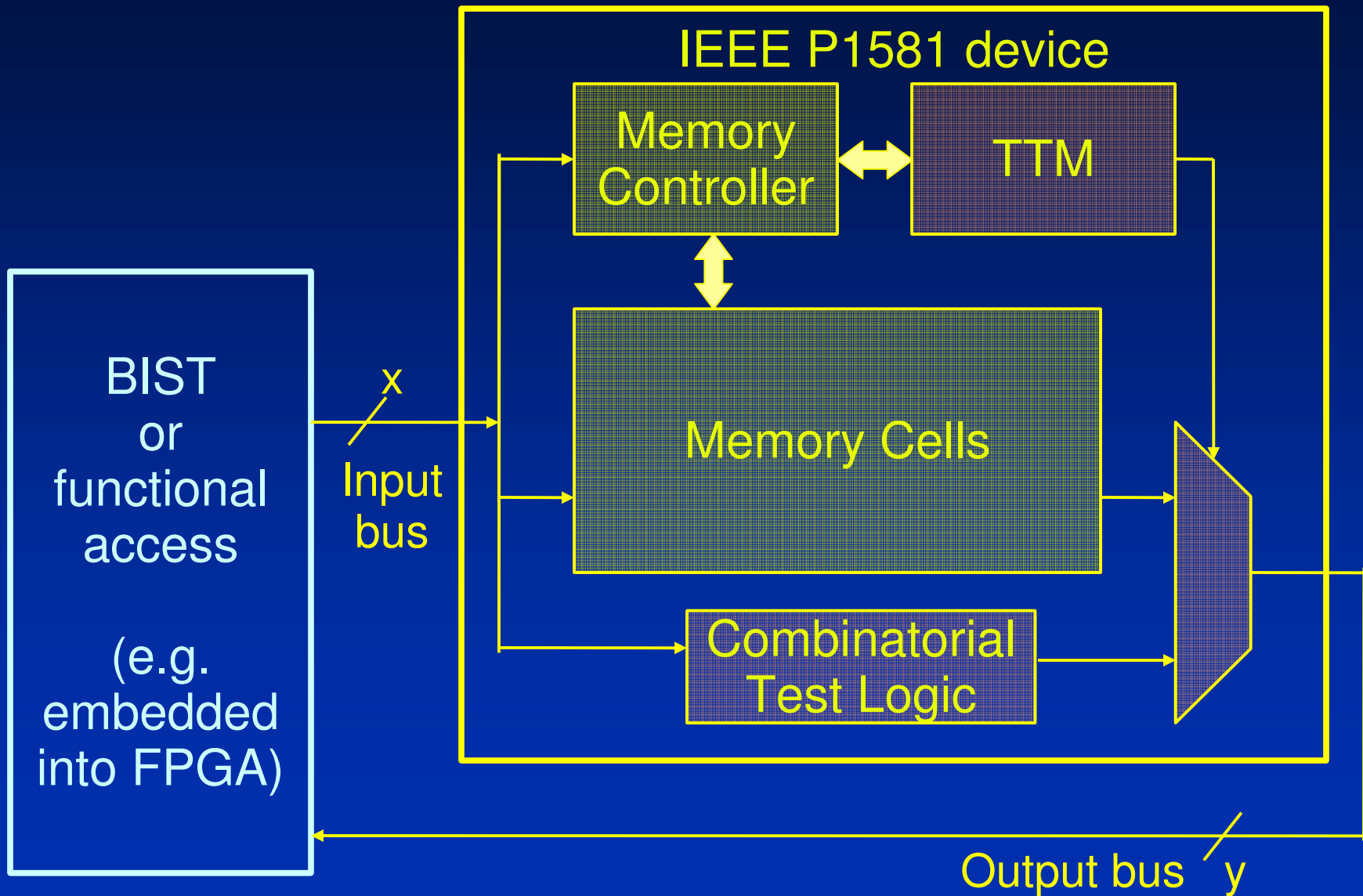
# IEEE P1581 principle



# IEEE P1581 principle



# IEEE P1581 principle



# Benefits

- For User:
  - No dedicated test pins required
  - Small test pattern file, shorter test time
  - All memory types can be supported
  - No dynamic requirements
  - Test patterns can be driven from BSCAN device, ICT, functional logic
  - Patterns can be generated by ATPG

# Benefits

- For Chip Manufacturer:
  - No dedicated test pins required
  - Reduced test logic (vs. 1149.1)
  - Only one series of devices need to be supported (if P1581 satisfies customer requirements)

# Conclusion

- IEEE P1581:
  - Enables new test applications
  - Improves existing test applications
  - Simple implementation, little overhead
  - Simple test pattern (resulting in small test programs)
- P1581 working group is soliciting input from Chip vendors

***<http://grouper.ieee.org/groups/1581/>***